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| ART UNIT | PAPER NUMBER |
|---|---|
| 2121 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/670,976 | FONTANA ET AL. | |
| | Examiner | Art Unit | |
| | Sergey Datskovskiy | 2121 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-18 have been submitted for examination.

2. Claims 1-18 have been rejected.

### *Specification*

3. The disclosure is objected to because of the following informalities: a printing error that has resulted in missing or badly visible letter "e" in multiple places throughout the specification (for example, in the last lines of pages 1 and 2).

Appropriate correction is required.

### *Claim Objections*

4. Claims 5, 9, 10, 12, 13 and 17 are objected to because of the following informalities: a missing letter "e" in the first line of each of the mentioned claims. Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claimed system and method for balancing and optimizing component methods is not tangible since it does not contain any structural limitations that would define it as a tangible device or a method of using such device

and producing real-world results instead of being just an abstract algorithm. One way to overcome this rejection would be to specify that the methods are implemented on a computer or to have a software product stored on a computer readable medium that runs the specified method when being executed on a computer. Furthermore, "methods" referred to in claims 1-3 represent an abstract term. A conventional meaning of "method" is a way of doing something, thus claims 1-3 are directed towards a manipulation of abstract ideas. Abstract ideas (see Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759) or mere manipulation of abstract ideas (see Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58) are not patentable.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 12, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Collins ("Parallel and Sequential Job Scheduling in Heterogeneous Clusters: A Simulation Study using Software in the Loop").

**Claim 1**

Collins teaches a system for component balancing in the processing of multiple applications (Abstract, disclosed as job scheduling in a parallel computing environment) comprising:

(a) means to establish and maintain response time goals for methods (page 3, section 2.2, lines 1-6 disclose choosing and weighting a metric of performance according to the values and priorities of the users. Response time goals are maintained by Parallel Job Scheduler (PJS, see page 5, chapter 3) that maintains the execution times in a database (page 7, lines 14-18));

(b) means to delay other associated methods to optimize the processing of selected more significant methods (priority scheduling, page 15, chapter 5.3, paragraph 2).

**Claim 2**

Collins teaches the system of claim 1 which includes:

(c) means for sensing when an increased load is occurring in order to increase said delay applied to less-significant methods (resource-monitoring tool, page 6, second paragraph; page 18, last paragraph discloses an ability to preempt low-priority jobs, *i.e.* increase their scheduling delay by running other jobs first).

**Claim 3**

Collins teaches the system of claim 2 which includes:

(d) means for sensing when said load is decreasing in order to reduce the delay time applied to other associated methods (resource-monitoring tool, page 6, second paragraph; page 12, first paragraph describes running scheduled jobs in parallel when available resources allow it).

**Claim 13**

Collins teaches in a component balancer system, a method for optimizing the processing of component-based applications (Abstract, disclosed as job scheduling in a parallel computing environment), comprising the steps of:

(a) securing a list of applications to be optimized (page 7, third paragraph from the bottom, disclosed as a list of jobs in job queues);

(b) prioritizing said list according to a priority assigned to each application (priority scheduling, page 15, chapter 5.3, paragraph 2);

(c) accessing and capturing all or user selected components associated with said applications (page 7, paragraph 4);

(d) analyzing which methods of which component should be optimized (page 9, chapter 4, first paragraph; analysis is done during the loop simulation).

**Claim 14**

Collins teaches the method of claim 13 wherein step (d) includes the step of:

(d1) automatically optimizing the processing sequence of said applications (page 12, lines 10-11; scheduling algorithm is designed to optimize performance by optimizing the processing sequence).

**Claim 15**

Collins teaches the method of claim 13 wherein step (d) includes the step of:

(d2) manually optimizing the processing sequence of said applications (optimization can be done manually by setting the priorities before scheduling, page 15, chapter 5.3, paragraph 2).

7. Claims 4-11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Snelick ("S-Check: a Tool for Tuning Parallel Programs").

**Claim 4**

Snelick teaches a method for balancing and optimizing the processing of component methods (disclosed as a software that optimizes parallel programs, see page 107, Abstract) comprising the steps of:

(a) selecting component methods to gather runtime data from selected components (disclosed as selecting test points, see page 109, chapter 3.1, first paragraph);

(b) calculating statistical metrics between pairs of methods (A,B,C,...N) (page 108, Figure 1, steps 4 and 5, bottom paragraph);

(c) using said statistical significance tests on said metrics to select certain methods for optimization and delay in processing (optimization is disclosed by automatically determining the appropriate delay values, see page 110, left column, last whole paragraph).

**Claim 5**

Snelick teaches the method of claim 4 which includes the step of:

(d) establishing a goal of specified response time for each method (A,B,C,...N) selected from step (c) (page 109, right column, lines 3-8).

**Claim 6**

Snelick teaches the method of claim 5 wherein step (d) includes the steps of:

(d1) targeting specific groups of methods for delay (page 109, Figure, chapter 3.1, lines 7-9);

(d2) setting specified response times as a goal for said specific groups (page 109, right column, lines 3-8, response times can be set for a selected section of code).

**Claim 7**

Snelick teaches the method of claim 6 wherein step (d) includes the step of:

(d3) establishing a response time goal for each method from a setting of no delay in a method, to a maximum delay in a method (page 108, left column, lines 3-8, delays can be turned off; delays can be set to any maximum value (page 110, left column, last whole paragraph)).

**Claim 8**

Snelick teaches the method of claim 7 which includes the step of :

(i) graphically displaying individual response time for optimized methods against the response time goal set for a method (page 110, chapter 3.4).

**Claim 9**

Snelick teaches in a component balancer system, a process for optimizing the sequence of processing component-based applications (disclosed as a software

that optimizes parallel programs, see page 107, Abstract). comprising the steps of:

(a) selecting several methods (for example, A,B,C, . . N) to be conditioned for analysis (disclosed as selecting test points, see page 109, chapter 3.1, first paragraph);

(b) gathering runtime data from said selected methods in order to find statistical operating significance between selected pairs (AB, BA, AC, CA, BC, CB,... of methods (page 108, Figure 1, step 3, bottom paragraph);

(c) collecting data to get a representative workload involving said pairs (AB, BA, AC, CA, BC. CB,...) of said selected methods (page 108, Figure 1, step 4, bottom paragraph);

(d) establishing an analysis report to determine when said method pairs (AB, BA, AC, CA, BC, CB, are processed to determine the average response time for processing when methods A,B,C,... N are run singly (non-overlapped) and when method pairs are run overlapped as AB, BA, AC, CA, BC, CB, ... (page 108, Figure 1, step 5, bottom paragraph)

**Claim 10**

Snelick teaches the method of claim 9 which includes the steps of:

(e) calculating a statistical number (F-value) which indicates the variance between average non-overlapped response times for A,B,C. . . .N and average

response times for overlapped pairs of methods AB. BA, AC. CA, BC, CB, ... (page 108, Figure 1, step 4, bottom paragraph)

(f) inquiring if the deviation in response times is below a threshold or if the average response time is below t milliseconds (disclosed as effects calculated in step 4 on page 108, a threshold is disclosed as a value measured in standard errors (SEs) in page 110, chapter 3.4, lines 4-11);

(g) selecting, above a threshold or an average response time, method calls having a deviation greater than t milliseconds (page 111, sensitivity analysis, Table 1, left column, last whole paragraph);

(h) optimizing those method calls indicating a deviation greater than a threshold n involving an average response time greater than t milliseconds (page 111, Table 1, right column, first paragraph).

**Claim 11**

Snelick teaches the method of claim 10 wherein step (h) includes the step of:

(hl) delaying the processing of one method in an overlapped pair of methods (page 108, lines 6-8, delays are disclosed to simulate adjustments in code efficiency, therefore, it is inherent to optimize the method by making such delays permanent).

**Claim 16**

Snelick teaches a component balancer system for setting and managing response time goals for the processing of multiple component-based application

methods (A, B, C, N) (disclosed as a software that optimizes parallel programs, see page 107, Abstract) comprising:

(a) means to discover and capture applications, machines and components to be processed using a component runtime conditioner (CRC) (page 107, chapter 2, disclosed as using Synthetic-Perturbation Screening in S-Check program, conditions runtime by employing artificial delays placed within segments of a parallel program);

(b) means to analyze pairs of methods (AB, BA, AC. CA. BC, CB) to determine which method response times are affected by other methods (page 108, Figure 1, steps 4 and 5, bottom paragraph);

(c) means to select those method pairs which show a substantial variance between the non-overlapped and the overlapped response times during the period involved with means (b) to analyze pairs (page 110, GUI means from chapter 3.4);

(d) means to optimize the processing of selected method pairs (page 109, left column, first whole paragraph, S-Check is a software tool that can optimize pairs of methods by changing their delay values);

(e) means to apply delays in the processing of one associated method of a method pair (page 108, Figure 1, step 2, bottom paragraph; delays are added through the parallel code).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snelick ("S-Check: a Tool for Tuning Parallel Programs").

**Claim 17**

Snelick does not expressly disclose the system of claim 16 where said means (e) to condition delays includes:

(e1) means to calculate said delay as a delay parameter using a fuzzy logic method to optimize said processing.

However, Examiner takes Official Notice that using fuzzy logic is well known in the art of computer programming.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a fuzzy logic method in calculating a delay parameter in order to simplify the user interface by replacing exact numbers with fuzzy expressions since Examiner takes official notice that using fuzzy logic is well known in the art of computer programming.

**Claim 18**

Snelick teaches the system of claim 17 which includes:

(e2) means to adjust said delay increment according to the load on the system as sensed by the number of calls per second (page 108, left column, lines 3-12. Delays are set according to the run time which is inherently affected by the load on the system. The limitation about measuring load in calls per second has not been given any patentable weight since it has no effect on the resulting process).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Underwood (US Patent No. 6,523,027) teaches interfacing servers in a Java based e-commerce architecture. Clark et al. (US App. No. 2005/0081157) teaches a user interface to display and manage an entity and associated resources. Fong et al. (US Patent No. 6,904,593) teaches a method of administering software components using asynchronous messaging in a multi-platform, multi-programming language environment. Barnett et al. (US Patent No. 6,922,832) teaches execution of dynamic services in a flexible architecture for e-commerce. Chris Rees ("Microsoft Application Center 2000 Component Load Balancing Technology Overview") teaches a component load balancing application.

**Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sergey Datskovskiy whose telephone number is (571) 272-8188. The examiner can normally be reached on Monday-Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight, can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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